IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

AVM TECHNOLOGIES, LLC, a Delaware Limited Liability Company	:	
Plaintiff,	:	
v.	:	Civil Action No. 10-610-RGA
INTEL CORPORATION, a Delaware Corporation	:	
Defendant.	:	

MEMORANDUM OPINION

Richard K. Herrmann, Mary B. Matterer, MORRIS JAMES LLP, Wilmington, DE; Edward W. Goldstein, Alissa Lipski, Gregg Goldstein, Harry Laxton Jr. (argued), GOLDSTEIN & LIPSKI, PLLC, Houston, TX; Matthew C. Lapple (argued), LAPPLE IP LAW, P.C., Irvine, CA.

Attorneys for Plaintiff AVM Technologies, LLC.

Richard L. Horowitz, David E. Moore, POTTER ANDERSON & CORROON LLP, Wilmington, DE; William F. Lee (argued), Lauren B. Fletcher, WILMER CUTLER PICKERING HALE AND DORR LLP, Boston, MA; David C. Marcus, WILMER CUTLER PICKERING HALE AND DORR LLP, Los Angeles, CA.

Attorneys for Defendant Intel Corporation.

March 30, 2012

ANDREWS, U.S. DISTRICT JUDGE:

Plaintiff AVM Technologies, LLC filed this patent infringement action against Defendant Intel Corporation on July 16, 2010. (D.I. 1). AVM alleges that Intel infringes U.S. Patent No. 5,859,547 ("the '547 Patent"). (D.I. 1). The '547 Patent, entitled "Dynamic Logic Circuit," claims an improved dynamic logic circuit "that has increased speed and reduced power." '547 Patent at col. 2 ll. 64-65. Additionally, the "power and speed of the circuit are substantially constant regardless of the number of inputs the circuit contains." *Id.* at col. 2 ll. 65-67. Presently before the Court is the matter of claim construction. Briefing on claim construction was completed on March 22, 2011, and the Court held a *Markman* hearing on January 27, 2012.[1] Seven terms are in dispute and Intel asserts that an additional four terms are not amenable to construction because they are indefinite.

I. CLAIM CONSTRUCTION

Claim construction is a question of law. *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 977-78 (Fed. Cir. 1995), *aff'd,* 517 U.S. 370, 388-90 (1996). When construing patent claims, a court considers the literal language of the claim, the patent specification and the prosecution history. *Id.* at 979. Of these sources, the specification is "always highly relevant to the claim construction analysis. Usually it is dispositive; it is the single best guide to the meaning of a disputed term." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312-17 (Fed. Cir. 2005) (citing *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)). However, "[e]ven when the specification describes only a single embodiment, the claims of the patent will

---

[1] The case was stayed between April 2011 and October 2011 to enable AVM to engage new counsel after AVM's counsel withdrew.

not be read restrictively unless the patentee has demonstrated a clear intention to limit the claim scope using 'words or expressions of manifest exclusion or restriction.'" *Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 906 (Fed. Cir. 2004) (quoting *Teleflex, Inc. v. Ficosa N. Am. Corp.*, 299 F.3d 1313, 1327 (Fed. Cir. 2002)).

A court may consider extrinsic evidence, including expert and inventor testimony, dictionaries and learned treatises, in order to assist it in understanding the underlying technology, the meaning of terms to one skilled in the art and how the invention works. *Phillips*, 415 F.3d at 1318-19; *see also Markman*, 52 F.3d at 979-80. However, extrinsic evidence is considered less reliable and less useful in claim construction than the patent and its prosecution history. *Phillips*, 415 F.3d at 1318-19 (discussing "flaws" inherent in extrinsic evidence and noting that extrinsic evidence "is unlikely to result in a reliable interpretation of a patent claim scope unless considered in the context of intrinsic evidence").

In addition to these fundamental claim construction principles, a court should also interpret the language in a claim by applying the ordinary and accustomed meaning of the words in the claim. *Envirotech Corp. v. Al George, Inc.*, 730 F.2d 753, 759 (Fed. Cir. 1984). If the patent inventor clearly supplies a different meaning, however, then the claim should be interpreted according to the meaning supplied by the inventor. *Markman*, 52 F.3d at 980. If possible, claims should be construed to uphold validity. *In re Yamamoto*, 740 F.2d 1569, 1571 (Fed. Cir. 1984).

A. Claim Terms with Agreed-Upon Claim Constructions

The parties agreed upon the constructions of various terms used in the '547 Patent, and the Court accepts them as detailed below for purposes of this litigation.

Claim Term or Phrase:	"coupled to"
Agreed-Upon Construction:	connected to, directly or through intervening elements
Claim Term or Phrase:	"coupled between"
Agreed-Upon Construction:	connected between, directly or through intervening elements
Claim Term or Phrase:	"couplable to"
Agreed-Upon Construction:	capable of being connected
Claim Term or Phrase:	"coupling"
Agreed-Upon Construction:	connected, either directly or through intervening elements
Claim Term or Phrase:	"anti-float circuit"
Agreed-Upon Construction:	a circuit used to prevent the precharge node from floating or otherwise losing the current state of circuit
Claim Term or Phrase:	"precharge node"
Agreed-Upon Construction:	the output node of the dynamic logic circuit

B. Claims in Dispute

1. "dynamic logic circuit"

Claims 1-7, 9, 12-14, 16, 18, and 21 of the '547 Patent are each directed to a "dynamic logic circuit" (or a method of using a "dynamic logic circuit") that includes a precharge transistor, an evaluation transistor, and a logic block.

AVM's Proposed Construction:	ordinary and customary meaning, *i.e.*, "a circuit that is precharged and subsequently performs a logical function"
Intel's Proposed Construction:	a dynamic circuit that implements a logic function, rather than a memory function
Court's Construction:	a dynamic circuit that implements a logic function

AVM argues that the term "dynamic logic circuit" does not need to be construed because

the term is found in the preambles of the asserted claims and a preamble is not limiting where the claims at issue recite structurally complete inventions. AVM, thus, proposes that the term "dynamic logic circuit" can be understood by its ordinary and customary meaning, *i.e.*, "a circuit that is precharged and subsequently performs a logical function." (D.I. 56 at 7-8).

Intel argues that the term "dynamic logic circuit" is limiting and, therefore, the term must be construed. Intel agrees with AVM that a "dynamic logic circuit" performs a logic function but proposes that the term should be construed to exclude the performance of a memory function. Intel also asserts that AVM's proposed construction is wrong because it would require the entire "dynamic logic circuit" to be precharged. (D.I. 54 at 6-7).

The Court construes the term "dynamic logic circuit" to mean "a dynamic circuit that implements a logic function." First, the term must be construed because the preamble is limiting. "[W]hen the limitations in the body of the claim rely upon and derive antecedent basis from the preamble, then the preamble may act as a necessary component of the claimed invention." *Bicon, Inc. v. Straumann Co.*, 441 F.3d 945, 952 (Fed. Cir. 2006). The term "dynamic logic circuit" in claim 1 provides the antecedent basis for limitations in the body of several claims. Claims 6, 10, 11, and 19 are examples of claims where the term "dynamic logic circuit" appears in both the preamble and body of the claim.[2] Because the term appears in the body of the claim, it refers back and must be a limitation.

Absent a "clear disavowal" based on "expressions of manifest exclusion or restriction" in the specification, it would be improper to construe the term "dynamic logic circuit" as excluding memory functions. *See Teleflex*, 299 F.3d at 1325. Because the '547 Patent contains no such

---

[2] AVM is not asserting claim 19 in this action. (D.I. 133).

disavowal, the term "dynamic logic circuit" cannot be construed to exclude logic functions that could also be characterized as memory functions.[3]

2. "dynamic logic block" or "logic block"

The "dynamic logic block" is a component of the "dynamic logic circuit" as described in Claim 1. '547 Patent, col. 8 ll. 47-48.

AVM's Proposed Construction:	a circuit block that implements a logic function of the dynamic logic circuit
Intel's Proposed Construction:	a circuit block that implements the logic function of the dynamic logic circuit
Court's Construction:	a circuit block that implements the logic function of the dynamic logic circuit

The specification provides that: "The logic block is so named because it determines the logical function of the dynamic logic circuit. The logic block includes one or more input transistors that can be arranged in any configuration to provide a desired logic function." '547 Patent, col. 4 ll. 52-56. Intel cites to the former sentence in support of its proposed construction, while AVM cites to the latter sentence in support of its proposed construction.

The Court construes the term "dynamic logic block" or "logic block" as "a circuit block that implements the logic function of the dynamic logic circuit." The specification defines the term "logic block" to require implementing the particular logic function of the "dynamic logic circuit." '547 Patent, col. 4 ll. 52-53. Although the sentence in the specification to which AVM cites provides that the input transistors can be arranged to provide a desired logic function, the

---

[3] If a person of ordinary skill in the art would understand logic functions and memory functions to be mutually exclusive categories, then the Court's construction is consistent with that understanding.

logic block performs only one logic function once the transistors are arranged, a point which AVM conceded at oral argument. (D.I. 135 at 32-33).

3. "evaluation transistor"

Each claim requires the "dynamic logic circuit" to include an "evaluation transistor."

AVM's Proposed Construction:	a transistor that functions to isolate the precharge node from the logic block and is used to control when the precharge node may discharge
Intel's Proposed Construction:	a transistor that is connected to a clock signal, rather than a data signal, and is used to control when the precharge node may discharge
Court's Construction:	a transistor that is connected to a clock signal and is used to control when the precharge node may discharge

Both parties agree that an "evaluation transistor" controls when the precharge node may discharge. They disagree, however, whether the term "evaluation transistor" requires a transistor that isolates the precharge node from the logic block and whether the claimed "evaluation transistor" must be connected to a clock signal, rather than a data signal.

AVM argues that the '547 Patent consistently describes the evaluation transistor's function as "to isolate the precharge node from the logic block" to prevent power from passing from the precharge node to the logic block. AVM, thus, argues that its proposed construction captures the essential function of the "evaluation transistor" and is consistent with the term's ordinary meaning. (D.I. 56 at 9).

Intel argues that, at the time the application for the '547 Patent was filed, evaluation transistors were well known in the art as clocked transistors used to control when charge could be pulled off the precharge node. Intel also argues that defining "evaluation transistor" to require isolation would render other claim limitations superfluous. (D.I. 54 at 11, 14).

The Court construes the term "evaluation transistor" to mean "a transistor that is connected to a clock signal and is used to control when the precharge node may discharge." The '547 Patent consistently describes the "evaluation transistor" as being connected to a clock signal. The claims expressly refer to this connection between the "evaluation transistor" and the clock signal. *See, e.g.*, '547 Patent col. 9 ll. 1-3 (claim 6: "A clock signal node coupled to the gates of the precharge and evaluation transistors for receiving a clock signal"); *id.* at col. 9 ll. 38-42 (claim 12: "an evaluation transistor having . . . the gate terminal coupled to a clock signal node"). The specification also repeatedly provides that the "evaluation transistor" is connected to a clock signal. *See, e.g.*, '547 Patent at col. 1 ll. 20-51 & Fig. 1A (evaluation transistor 115 connected to clock signal 123); *id.* at col. 4 ll. 33-35 ("The gate 330 [of evaluation transistor 306] is coupled to a clock node 334 for receiving a clock signal").

AVM's proposed construction requiring that the "evaluation transistor isolate[] the precharge node from the logic block" contradicts the '547 Patent's own use of the term "evaluation transistor." In describing the prior-art circuit in Figure 1A, the specification identifies transistor 114 as an "evaluation transistor." '547 Patent col. 1 ll. 42-44. Evaluation transistor 114, however, is not located between logic block 116 and precharge node 124 and, therefore, cannot function to isolate the precharge node from the logic block. In addition, defining "evaluation transistor" to require isolation would render other claim limitations superfluous. Claims 1, 19, and 22 each recite "an evaluation transistor between the dynamic logic block and the precharge transistor." *See* '547 Patent col. 8 ll. 50-51, col. 10 ll. 15-16, col. 10 ll. 52-53. To the extent the claims require the "evaluation transistor" to perform an isolation function, that requirement comes from the claim limitations describing the evaluation transistor

as located between the logic block and precharge node – not from the term "evaluation transistor."

4. "precharge transistor"

Each claim requires the "dynamic logic circuit" to include a "precharge transistor."

AVM's Proposed Construction:	transistor that charges a precharge node and not the logic block during the precharge phase
Intel's Proposed Construction:	a transistor that is connected to a clock signal, rather than a data signal, and charges the precharge node
Court's Construction:	a transistor that is connected to a clock signal and charges the precharge node

Both parties agree that the "precharge transistor" charges the precharge node. They disagree, however, whether the "precharge transistor" may charge the logic block during the precharge phase and whether the "precharge transistor" must be connected to a clock signal, rather than a data signal.

AVM argues that "the '547 Patent teaches that the precharge transistor should be configured to charge only the precharge node during the precharge phase . . . [to] prevent[] the logic block from siphoning charge from the precharge node and consuming more power." AVM, thus, argues that its proposed construction captures the essential function of the "precharge transistor" and comports with the manner in which the inventors described their invention. (D.I. 56 at 11).

Intel argues that, at the time the application for the '547 Patent was filed, precharge transistors were well known as clocked transistors used to charge the precharge node. Intel also argues that defining "precharge transistor" to require that it not charge the logic block during the precharge phase directly contradicts the '547 Patent. (D.I. 54 at 9-10).

The Court construes the term "precharge transistor" to mean a "transistor that is connected to a clock signal and charges the precharge node." The '547 Patent indicates that the "precharge transistor" is connected to a clock signal either directly or indirectly through a delay. The claim language specifically refers to this connection between the "precharge transistor" and the "clock signal." *See, e.g.*, '547 Patent, col. 9 ll. 10-12 (claim 7: "the delay is coupled between the clock signal node and the gate of the precharge transistor"); *id.* at col. 9 ll. 44-45 (claim 12: "a delay coupled between the clock signal node and the gate terminal of the precharge transistor"). The specification also confirms that the "precharge transistor" must be connected to a clock signal. In describing the prior art, the specification explains that "[a] clock signal path 123 is coupled to the precharge and evaluation transistors [112 and 114, respectively]." *Id.* at col. 1 ll. 28-30 & Fig. 1A. Similarly, each disclosed embodiment of the claimed invention includes a "precharge transistor" that is connected to a delayed clock signal and not a data signal. *See, e.g.*, *id.* at col. 5 ll. 12-16 & Fig. 3A.

AVM's proposed construction, which requires that the "precharge transistor" *not* charge the logic block during the precharge phase, directly contradicts the '547 Patent. In describing the prior art circuit in Figure 1A, the specification identifies transistor 112 as a "precharge transistor." *See* '547 Patent col. 1 ll. 22-23. The specification then states: "During the precharge phase, [precharge] transistor 112 is active . . . charging a precharge node 124 and the logic block 116 to a logic high voltage level." *Id.* at col. 1 ll. 34-37. The specification thus uses the term "precharge transistor" to refer to a transistor that charges the logic block during the precharge phase.

5. "a delay"

Two independent claims of the '547 Patent require the "dynamic logic circuit" to include a "delay." Claim 1 recites "a delay coupled to the precharge transistor for simultaneously activating the precharge and evaluation transistors." '547 Patent, col. 8 ll. 52-54. Similarly, Claim 12 recites "a delay coupled between the clock signal node and the gate terminal of the precharge transistor." *Id.* at col. 9 ll. 43-44.

AVM's Proposed Construction:	circuit that postpones deactivation of the precharge transistor until after activation of the evaluation transistor
Intel's Proposed Construction:	no construction required
Court's Construction:	a circuit element that delays the clock signal to the precharge transistor

AVM argues that the patent refers to "'delay' as a physical component of the circuit and one that causes the precharge transistor to remain 'on' or 'activated' for a period of time while the evaluation transistor is also 'on.'" Because the delay circuit delays the timing signal to the precharge transistor, the precharge transistor deactivates later than if it received the timing signal without a delay present. (D.I. 56 at 13).

Intel initially argued that it was unnecessary to construe the term "delay" because a jury would understand it as a non-technical term. (D.I. 54 at 15). At oral argument, however, Intel proposed that "delay" be construed as "a circuit element that delays the clock signal to the precharge transistor." (D.I. 133 at 142-43).

The Court construes the term "delay" to mean "a circuit element that delays the clock signal to the precharge transistor." The specification provides: "The delay 308 delays the clock signal so that the signal at the gate 312 of the precharge transistors receives a phase-shifted clock

signal." '547 Patent at col. 5 ll. 13-15. AVM's proposed construction of the term "delay" would render the term "for simultaneously activating" in claim 1 redundant. If AVM's proposed construction were adopted and substituted for "a delay," Claim 1 would read: "a circuit that postpones deactivation of the precharge transistor until after activation of the evaluation transistor coupled to the precharge transistor for simultaneously activating the precharge and evaluation transistors."

6. "for simultaneously activating"

Claim 1 of the '547 Patent recites that the "dynamic logic circuit" includes "a delay coupled to the precharge transistor for simultaneously activating the precharge and evaluation transistors."

AVM's Proposed Construction:	for causing to be on concurrently for a portion of the evaluation phase
Intel's Proposed Construction:	for causing to be on concurrently
Court's Construction:	for causing to be on at the same time

The specification demonstrates that the precharge and evaluation transistors are "simultaneously activated" when they are on at the same time. '547 Patent, col. 6 ll. 45-49. ("FIG. 4E shows an overlap period during which the precharge transistor and the evaluation transistor are both simultaneously activated."). The parties agree that the phrase requires that the precharge and evaluation transistors to be on at the same time. They disagree, however, whether the term requires that this activation occur "for a portion of the evaluation phase."

The Court construes the term "for simultaneously activating" to mean "for causing to be on at the same time." AVM's proposed construction would narrow improperly the plain meaning of the claim language by importing a limitation from the preferred embodiment. *See, e.g.,*

Liebel-Flarsheim Co. v. Medrad, Inc., 358 F.3d 898, 913 (Fed. Cir. 2004) (refusing to limit "opening" to a specific location, because "it is improper to read limitations from a preferred embodiment . . . into the claims"); *Comark Commc'ns, Inc. v. Harris Corp.*, 156 F.3d 1182, 1187 (Fed. Cir. 1998) (refusing to limit "video delay circuit" to the preferred embodiment, because "it is precisely against this type of claim construction that our prior case law counsels."). Conversely, other claim limitations do specify when the simultaneous activation must occur. For example, Claim 21 requires "that the precharge transistor is activated during a minor portion of the evaluation clock phase." '547 Patent, col. 10 ll. 44-46. Claim 1, which recites "simultaneously activating the precharge and evaluation transistors," contains no similar requirement.

C. Claim Terms That Intel Contends Are Not Amenable to Construction

Claim 6 requires the precharge transistor to be inactive "during a major portion of the evaluation phase." '547 Patent at col. 9 ll. 5-6. Claim 21 requires the precharge transistor to be inactive "during a major portion of the evaluation clock phase" and active "during a minor portion of the evaluation clock phase." Intel argues that these phrases are not amenable to construction because they are so vague in scope that they render the claims indefinite and, therefore, invalid under 35 U.S.C. § 112, ¶ 2. (D.I. 54 at 19-20). The Federal Circuit has made clear that the standard of indefiniteness is high. *See Praxair v. ATMI, Inc.*, 543 F.3d 1306, 1319 (Fed. Cir. 2008) (citing *Exxon Research & Eng'g Co. v. United States*, 265 F.3d 1371, 1375 (Fed. Cir. 2001)). "Because a claim is presumed valid, a claim is indefinite only if the 'claim is insolubly ambiguous, and no narrowing construction can properly be adopted.'" *Honeywell Int'l. Inc. v. Int'l Trade Comm'n.*, 341 F.3d 1332, 1338-39 (citing *Exxon*, 265 F.3d at 1375). In

addition, the Federal Circuit has recognized the term "majority" does not render a claim indefinite and can be construed. *Moore U.S.A., Inc. v. Standard Register Co.*, 229 F.3d 1091, 1106 (Fed. Cir. 2000).

1. "during a major portion of the evaluation phase"

Intel's Contention:	Renders claim 6 invalid for indefiniteness under 35 U.S.C. § 112, ¶ 2
AVM's Response:	One of ordinary skill in the art would understand the phrase "a major portion of the evaluation phase."
Court's Construction:	a period greater than 50% of the evaluation phase

The Court construes the term "during a major portion of the evaluation phase" to mean a period greater than 50% of the evaluation phase.

2. "during a major portion of an evaluation clock phase"

Intel's Contention:	Renders claim 21 invalid for indefiniteness under 35 U.S.C. § 112, ¶ 2
AVM's Response:	One of ordinary skill in the art would understand the phrase "a major portion of an evaluation clock phase."
Court's Construction:	a period greater than 50% of an evaluation clock phase

The Court construes the term "during a major portion of an evaluation clock phase" to mean "a period greater than 50% of an evaluation clock phase."

3. "during a minor portion of the evaluation clock phase"

Intel's Contention:	Renders claim 21 invalid for indefiniteness under 35 U.S.C. § 112, ¶ 2
AVM's Response:	One of ordinary skill in the art would understand the phrase "a minor portion of the evaluation clock phase."
Court's Construction:	a period less than 50% of the evaluation clock phase

The Court construes the term "during a minor portion of the evaluation clock phase" to mean "a period less than 50% of the evaluation clock phase."

The claim language shall be construed as set forth above.